

PATENT  
Attorney Docket 2777.4US (95-1024.3)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL740533713US

Date of Deposit with USPS: July 23, 2001

Person making Deposit: Jared Turner

APPLICATION FOR LETTERS PATENT

for

**FLIP CHIP TECHNIQUE FOR CHIP ASSEMBLY**

Inventor:  
Mirmajid Seyyedy

Attorney:  
James R. Duzan  
Registration No. 28,393  
TRASKBRITT, PC  
P.O. Box 2550  
Salt Lake City, Utah 84110  
(801) 532-1922

# FLIP CHIP TECHNIQUE FOR CHIP ASSEMBLY

## BACKGROUND OF THE INVENTION

[0001] Cross Reference to Related Applications: This application is a continuation of application Serial No. 09/392,153, filed September 8, 1999, pending, which is a divisional of application Serial No. 08/788,209, filed January 24, 1997, now U.S. Patent 6,221,753 B1, issued April 24, 2001.

[0002] Field of the Invention: The present invention relates to an apparatus and a method for connecting one substrate, such as a flip-chip type semiconductor die, to another substrate, such as a silicon wafer, printed circuit board, or other substrate (hereinafter referred to generally as a "substrate"). More particularly, the present invention relates to a semiconductor die having a raised bond pad attached to a substrate which also has raised bond pads aligned to make electrical contact with the die bond pad without attachment.

[0003] State of the Art: A flip chip is a semiconductor chip or die that has bumped terminations spaced around the active surface of the die and is intended for face-to-face attachment to a substrate or another semiconductor die. The bumped terminations of the flip chips are usually a "Ball Grid Array" ("BGA") configuration wherein an array of minute solder balls is disposed on an attachment surface of a semiconductor die, or a "Slightly Larger than Integrated Circuit Carrier" ("SLICC") configuration wherein an array of minute solder balls is disposed on an attachment surface of a semiconductor die similar to a BGA, but having a smaller solder ball pitch and diameter than a BGA.

[0004] The attachment of a flip chip to a substrate or another semiconductor involves aligning the solder balls on the flip chip with a plurality of contact points (configured to be a mirror image of the solder ball arrangement on the flip chip) on a facing surface of the substrate. A plurality of solder balls may also be formed on a facing surface of the substrate at the contact points. A quantity of liquid flux is often applied to the face of the chip and/or substrate, and the chip and substrate are subjected to elevated temperature to effect refluxing or soldering of the solder balls on the chip and/or corresponding solder balls on the substrate.

**[0005]** There are numerous variations to the standard flip chip attachment technique. For example, U.S. Patent 5,329,423 issued July 12, 1994 to Scholz relates to a demountable flip chip assembly comprising a first substrate having a contact site with a raised bump and a second substrate having a depression for a contact site. The raised bumps are pressed into the depressed areas to electrically and mechanically connect the first substrate to the second substrate without using reflowed solder. Thus, the first substrate can be removed from the second substrate without damaging either substrate.

**[0006]** U.S. Patent 5,477,086 issued December 19, 1995 to Rostoker et al. relates to a flip chip attachment technique involving forming a concave conductive bump on one substrate (such as the PCB) to receive and align the solder balls on the other substrate (such as the semiconductor die). The solder balls and/or the concave conductive bump are reflowed to fuse them together.

**[0007]** It is also known in the art that conductive polymers or resins can be utilized in place of solder balls. U.S. Patent 5,258,577 issued November 2, 1993 to Clements relates to a substrate and a semiconductor die with a discontinuous passivation layer. The discontinuities result in vias aligned with the contact points between the substrate and the semiconductor die. A resin with spaced conductive metal particles suspended therein is disposed within the vias to achieve electrical contact between the substrate and the semiconductor die. U.S. Patent 5,468,681 issued November 21, 1995 to Pasch relates to interconnecting conductive substrates using an interposer having conductive plastic filled vias.

**[0008]** Such flip chip and substrate attachments (collectively “electronic packages”) are generally comprised of dissimilar materials that expand at different rates on heating. The most severe stress is due to the inherently large thermal coefficient of expansion (“TCE”) mismatch between the plastic and the metal. These electronic packages are subject to two types of heat exposures: process cycles, which are often high in temperature but few in number; and operation cycles, which are numerous but less extreme. If either the flip chip(s) and/or substrate(s) are unable to repeatedly bear their share of the system thermal mismatch over its lifetime, the electronic package will fracture, thereby destroying the functionality of the electronic package.

**[0009]** As an electronic package dissipates heat to its surroundings during operation, or as the ambient system temperature changes, differential thermal expansions cause stresses to be generated in the interconnection structure (solder ball bonds) between the semiconductor die and the substrate. These stresses produce instantaneous elastic and, most often, plastic strain, as well as time-dependent (plastic and anelastic) strains in the interconnection structure, particularly at the weakest interconnection structure. Thus, the thermal expansion mismatch between chip and substrate will cause a shear displacement to be applied on each terminal which can fracture the solder connection.

**[0010]** The problems associated with thermal expansion match are also applicable to connections made with conductive polymers or resins. After curing, the polymers or resins become substantially rigid. The rigid connections are equally susceptible to breakage due to thermal expansion mismatch.

**[0011]** Therefore, it would be advantageous to develop an apparatus for connecting a first semiconductor die or substrate to a second semiconductor die or substrate in such a manner that electrical contact is made at the contact points but no mechanical attachment occurs at the contact point. Such a connection would eliminate the possibility of fractures occurring at the contact points.

## SUMMARY OF THE INVENTION

**[0012]** The present invention relates to an apparatus and a technique for connecting a first substrate to a second substrate wherein the first substrate has a plurality of raised bond pads which make electrical contact (without attachment) with a plurality of raised bond pads on the second substrate.

**[0013]** A preferred method for constructing the apparatus of the present invention comprises providing a first substrate having a plurality of leads on an active surface or within the first substrate. A plurality of conductive bumps which contacts the leads is formed on the active surface of the first substrate. The conductive bumps are preferably metallic, such as copper, aluminum, or the like, and are formed by any number of known industry techniques, such as photolithography (subtractive or additive etching), liquid photoresist, dry-film photoresist, silk

screening, or the like. The conductive bumps are also preferably flat on an upper surface of the conductive bumps.

[0014] A silicon wafer is preferred as the first substrate because the silicon wafer is usually very smooth and planar due to the chemical mechanical polishing (planarizing) or "CMP" step in silicon wafer production. A smooth and planar surface is preferred so that the conductive bumps are of even height across the silicon wafer.

[0015] A second substrate is provided which preferably also has a plurality of leads on an active surface or within the second substrate. A plurality of conductive bumps which contacts the leads is formed on the active surface of the second substrate in the same manner as described for the first substrate. The conductive bumps are preferably the same metallic material as the first substrate conductive bumps or at least a very similar metallic material. The conductive bumps are also preferably flat on a facing surface of the conductive bumps.

[0016] The second substrate is preferably a flip chip, such as a memory chip, a CPU, or a logic chip. Flip chips are generally manufactured with a plurality of bond pads on an active surface wherein each bond pad is connected to a lead. A facing surface of each bond pad has the conductive bump formed thereon.

[0017] A passivation layer is applied over the second substrate active surface. The passivation is preferably thicker than the height of the second substrate conductive bumps. The passivation layer is etched by any known industry standard technique to form vias to expose an active surface of the second substrate conductive bump. It is, of course, understood that, rather than etching the passivation layer, a masking technique could be employed, such as a silk screen, over the semiconductor die conductive pad facing surface when applying the passivation layer.

[0018] The apparatus of the present invention is completed by attaching the first substrate to the second substrate. The first substrate conductive bumps and the second substrate conductive bumps are aligned to be the mirror-image of one another, such that when the one substrate is flipped to attach to the other substrate component, each first substrate conductive bump contacts its respective second substrate conductive bump. A layer of adhesive is disposed between the passivation layer and the first substrate upper surface. When the first substrate is attached to the second substrate, an upper surface of the first substrate conductive bump and the

second substrate conductive bump upper surface come into electrical communication without being mechanically attached to one another. The layer of adhesive may be eliminated if a glob top or encapsulant is used to secure or encase the apparatus. It is, of course, understood that the passivation layer could be applied to the first substrate active surface, etched, and adhered to the second substrate active surface.

**[0019]** Thus with no mechanical attachment between the conductive bumps of the first substrate and the conductive bumps of the second substrate, thermal expansion will simply cause the conductive bumps to shift from side to side as the substrates expand or contract without losing electrical contact with one another. The preferred flat upper surfaces of both the first substrate conductive bumps and the second substrate conductive bumps maximize the potential contact surface of the conductive bumps as the substrates expand or contract.

**[0020]** During the assembly process, it is preferable to test the electrical contact of the conductive bumps between the first substrate and the second substrate while the adhesive is curing to fine tune for the best position and assure the functionality of the apparatus before the adhesive sets. When using a glob top or encapsulant, the electrical contact of conductive bumps should be tested prior to the application of the glob top or encapsulant.

**[0021]** Grooves on the facing surface of the first substrate and/or second substrate may be provided to assist in preventing or minimizing the movement of the substrates in relation to one another due to thermal expansion or other mechanical causes.

#### BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

**[0022]** While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

**[0023]** FIG. 1 is a side cross-sectional view of a first substrate component of the present invention;

**[0024]** FIG. 2 is a side cross-sectional view of a second substrate component of the present invention;

**[0025]** FIG. 3 is a side cross-sectional view of a first substrate/second substrate assembly of the present invention;

**[0026]** FIG. 4 is a side cross-sectional view of a first alternative first substrate/second substrate assembly of the present invention;

**[0027]** FIG. 5 is a side cross-sectional view of a second alternative first substrate/second substrate assembly of the present invention;

**[0028]** FIG. 6 is a side cross-sectional view of a third alternative first substrate/second substrate assembly of the present invention; and

**[0029]** FIG. 7 is a side cross-sectional view of a fourth alternative first substrate/second substrate assembly of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

**[0030]** FIG. 1 illustrates a first substrate component 100 of the present invention. The first substrate component 100 comprises a first substrate 102 having a plurality of leads 104 on a facing surface 106 of the first substrate 102. A conductive pad 108 is formed on a facing surface 110 of at least one substrate lead 104.

**[0031]** FIG. 2 illustrates a second substrate or flip-chip component 200 of the present invention. The flip-chip component 200 comprises a second substrate or semiconductor die 202 having a plurality of bond pads 204 on a facing surface 206 of the semiconductor die 202. Each bond pad 204 is connected to a trace lead 208 (shown by a dashed line) on a lower bond pad surface 210. A facing surface 212 of each bond pad 204 has a conductive pad 214 formed thereon. A passivation layer 216 is applied over the semiconductor die facing surface 206. The passivation layer 216 is etched by any known industry standard technique to form vias 218 to expose a facing surface 220 of the semiconductor die conductive pad 214. It is, of course, understood that, rather than etching the passivation layer 216, a masking technique could be employed, such as a silk screen, over the semiconductor die conductive pad facing surface 220 when applying the passivation layer 216.

**[0032]** FIG. 3 illustrates a first substrate/second substrate assembly 300 of the present invention. The first substrate/second substrate assembly 300 is a combination of the first

substrate component 100 of FIG. 1 and the second substrate or flip-chip component 200 of FIG. 2; therefore, components common to FIGS. 1, 2, and 3 retain the same numeric designation. The substrate conductive pads 108 and the semiconductor die conductive pads 214 are aligned to be the mirror-image of one another, such that when the flip-chip component 200 is flipped to attach to the first substrate component 100, each substrate conductive pad 108 contacts its respective semiconductor die conductive pad 214. Thus, the substrate/flip-chip assembly 300 is constructed by flipping the flip-chip component 200 and attaching the flip-chip component 200 to the first substrate component 100. A layer of adhesive 302 is disposed between the passivation layer 216 and the first substrate facing surface 106. When the flip-chip component 200 is attached to the first substrate component 100, a facing surface 304 of the first substrate conductive pad 108 and the semiconductor die conductive pad facing surface 220 come into electrical communication without being attached to one another. It is, of course, understood that the passivation layer could be applied to the first substrate active surface, etched, and adhered to the second substrate active surface.

**[0033]** FIG. 4 illustrates a first alternative first substrate/second substrate assembly 400 of the present invention. The first alternate first substrate/second substrate assembly 400 is similar to the first substrate/second substrate assembly 300 of FIG. 3; therefore, components common to FIG. 3 and FIG. 4 retain the same numeric designation. The first alternative first substrate/second substrate assembly 400 differs from the first substrate/second substrate assembly 300 in that the second substrate or flip-chip component 200 is specifically a substrate with the conductive pad 214 formed on a substrate lead 408, rather than on a flip chip type bond pad 204 connected to a trace lead 208 shown in FIG. 3. The first alternative first substrate/second substrate assembly 400 also differs from the first substrate/second substrate assembly 300 in that the passivation layer 216 is first applied to first substrate facing surface 106, then a layer of adhesive 402 is disposed between the passivation layer 216 and the second substrate 202.

**[0034]** FIG. 5 illustrates a second alternative first substrate/second substrate assembly 500 of the present invention. The second alternate first substrate/second substrate assembly 500 is similar to the first substrate/second substrate assembly 300 of FIG. 3; therefore, components



common to FIG. 3 and FIG. 5 retain the same numeric designation. The second alternative first substrate/second substrate assembly 500 differs from the first substrate/second substrate assembly 300 in that a glob top material 502 is used to attach the second substrate or flip-chip component 200 to the first substrate component 100, rather than using the layer of adhesive 302 shown in FIG. 3.

[0035] FIG. 6 illustrates a third alternative first substrate/second substrate assembly 600 of the present invention. The third alternate first substrate/second substrate assembly 600 is similar to the first substrate/second substrate assembly 300 of FIG. 3; therefore, components common to FIG. 3 and FIG. 6 retain the same numeric designation. The third alternative first substrate/second substrate assembly 600 differs from the first substrate/second substrate assembly 300 in that an encapsulant material 602 is used to substantially encase and attach the second substrate or flip-chip component 200 together with the first substrate component 100, rather than using the layer of adhesive 302 shown in FIG. 3.

[0036] FIG. 7 illustrates a fourth alternative first substrate/second substrate assembly 700 of the present invention. The fourth alternate first substrate/second substrate assembly 700 is similar to the first substrate/second substrate assembly 300 of FIG. 3; therefore, components common to FIG. 3 and FIG. 7 retain the same numeric designation. The fourth alternative first substrate/second substrate assembly 700 differs from the first substrate/second substrate assembly 300 in that a first plurality of grooves 702 is disposed on the facing surface 106 of the first substrate 102 and a second plurality of grooves 704 is disposed on the facing surface 206 of the second substrate 202 wherein the first plurality of grooves 702 intermesh with the second plurality of grooves 704 to assist in preventing or minimizing the movement of first substrate 102 and/or second substrate 202 due to thermal expansion or other mechanical causes.

\* \* \* \* \*

[0037] Having thus described in detail preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by

particular details set forth in the above description as many apparent variations thereof are possible without departing from the spirit or scope thereof.